FC7240Fxx Product Brief

[FC7240F2MDS]

The FC7240 product series extends the FC4150 family in the automotive industry with the Arm Cortex-M7 core at higher performance, larger memory, and ASILD rating. It also supports security requirements including the secure boot and EVITA full. The FC7240 is suitable for a wide range of applications in automotive.

Key Features

- 32-bit ARM® Cortex®-M7 core
- Up to 240 MHz execution speed
- Up to 2 MB PFlash, 128 KB DFlash, and 256 KB RAM
- Temp Grade1/-40°C to +125°C
- ISO 26262 ASIL-D support
- Package: LQFP-EP-176, -144, -100

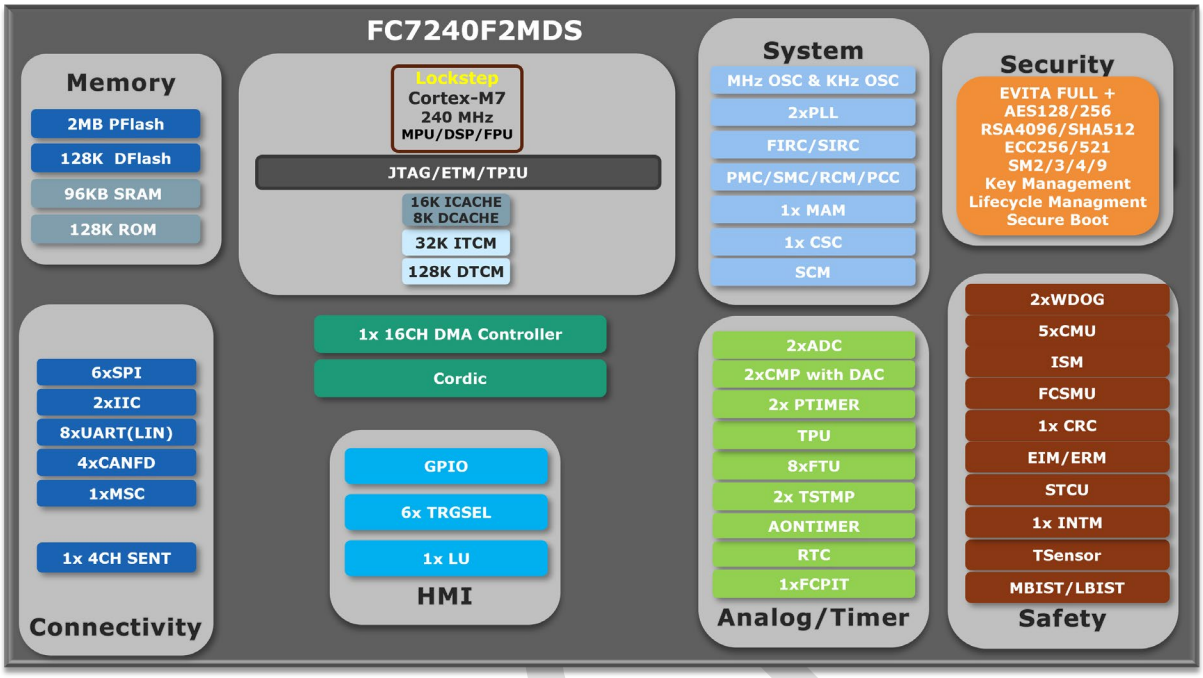
Target Applications

- Advanced Driver Assistant System (ADAS)
- Active suspension control system
- Motor control
- 800V/400V Battery Management System (BMS)
- Electric Power Steering (EPS)
- Electronic Stability Control (ESC)
- Anti-lock Brake System (ABS)

1 Block Diagram

The following figures show the block diagram of the FC7240 family.

Figure 1. FC7240F2MDS block diagram



2 Features

The FC7240 product series has the following features:

2.1 Overview

- **Operating Environment**
  - Voltage range: 3.0 V to 5.5 V
  - Ambient temperature range: -40°C to +125°C; junction temperature: -40°C to +150°C
- **Arm Cortex-M7 Core**
  - 240 MHz frequency with 3.23 Dhrystone MIPS per MHz
  - Armv7 Architecture and Thumb-2 ISA
  - Digital Signal Processing (DSP) instruction
  - Single-precision Floating Point Unit (FPU)
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Support Memory Protection Unit (MPU) with 16 regions
  - Each core has 16 KB ICACHE and 8 KB DCACHE
  - Each core has 64 KB ITCM, and 64KB DTCM0 and 64 KB DTCM1
- **One CM7 running core (CPU0)**: CPU0 with extra checker cores to form lockstep operation. The lockstep monitor also covers the CM7 AXI2AHB and ITCM/DTCM0&1 ECC logic.
- **CORDIC accelerator for mathematical operations such as angles**
- **Mailbox with up to 4 communication channels and 2 interrupt channels for on-chip CPU and HSM;** support the hardware semaphore function.
- **One Matrix Access Monitor (MAM)**, which monitors all on-chip matrix access, and supports watchdog timeout function for matrix access.
- **One Core System Control (CSC) module**; used for the stop mode related handle etc. control.
- **One System Control Module (SCM)**; used for the on-chip connection control, lock step control, CPU low power status, interrupt routing control, etc.
- **One Security Controller (SEC)**; used for on-chip debug/test mode/lifecycle-related control.
- **One 16-channel Direct Memory Access (DMA)** with selectable DMA sources.
- **Clock Sources**
  - 16 ~ 48 MHz Fast Oscillator (FOSC) with up to 50 MHz DC external input clock in bypass mode.
  - 32 kHz Slow Oscillator (SOSC)
  - 96 MHz Fast Internal RC Oscillator (FIRC96M)
  - 12 MHz Slow Internal RC Oscillator (SIRC12M)
  - 32 kHz Slow Internal RC Oscillator (SIRC32k)
  - Up to 400 MHz Phased Lock Loop (PLL0 and PLL1) with the reference clock from FIRC 48 MHz or FOSC.
- **Power Management**
  - Four power modes: RUN, WAIT, STOP and Standby. Optional 64 KB System RAM retention in standby mode.
- **Memory**
  - Up to 2 MB program flash memory with Address and Data Single-bit Error Correction and Double-bit Error Detection (SECDED).
  - Up to 128 KB data flash memory with Address and Data SECDED.
  - Up to 96 KB SRAM with Address and Data SECDED.

- 128 KB ROM with Address and Data SECDED, which contains CM7 core self-test/flash program & erase/ Hardware Secure Module (HSM) secure boot etc.

- **Analog**
  - Up to two 12-bit Successive Approximation (SAR) Analog-to-Digital Converters (ADCs) with up to 32 channel analog inputs per module
  - Up to two Analog Comparators (CMPs) with internal 8-bit Digital-to-Analog Converter (DAC)
- **Debug Functionality**
  - Serial Wire/JTAG Debug Port (SWJ-DP) combines
  - Data Watchpoint and Trace (DWT)
  - Instrumentation Trace Macrocell (ITM)
  - Embedded Trace Macrocell (ETM)
  - Trace Port Interface Unit (TPIU) with up to 16-bit
  - Flash Patch and Breakpoint (FPB) Unit
  - JTAG Test Access Port (TAP) and boundary scan support
- **Human-Machine Interface (HMI)**
  - Up to 152 GPIO pins with separated core interrupt support
  - Non-Maskable Interrupt (NMI)
  - GPIO interface with separated core control
- **Communications Interfaces**
  - Up to eight FC Universal Asynchronous Receiver/Transmitter (FCUART) modules with LIN support
  - Up to six FC Serial Peripheral Interface (FCSPI) modules; support 1/2/4 data lines and master/slave mode
  - Up to two FC Inter-Integrated Circuit (FCIIC) modules
  - Up to four FLEXCAN modules with optional CAN-FD support
  - One Micro Second Channel (MSC) module
  - One 4-channel Sent Edge Nibble Transmit (SENT) module
  - Up to six Trigger Selects (TRGSELs) for on-chip bus connection
  - One Lookup Unit (LU) module; supports 4 lookup tables
- **Security**
  - Hardware Secure Module (HSM) with crypto algorithms including AES/SM4/ECC/RAS/SHA/SM3/SM4/SM9
  - EVITA full capability
  - Support random number generation and pseudo random number generation
  - Key import/export management
  - Monotonic counter support
  - Support secure boot and non-secure boot mode
  - Support In-System Program (ISP) mode
- **Safety**
  - Up to five Clock Monitor Units (CMUs, 0-4) for all internal critical root clock source monitor
  - PMC with LVR/LVD/HVD etc. on internal generate supply and external supply protection
  - ECC with both address and data protection on ROM, flash and SRAM memories
  - One Memory Access Monitor (MAM) on the system memory, including the APB bridge (AFCB0 and AFCB1) etc. peripheral slots
  - One Cyclic Redundancy Check (CRC) module
  - Up to two internal Watchdogs (WDOGs) with window function

- One Error Injection Module (EIM) for ECC logic and lock step logic check
- One Error Reporting Module (ERM) for ECC-related monitor errors
- One Fault Control and Safety Management Unit (FCSMU) for on-chip error handling and optionally outputting the chip status to external pins
- LockStep Monitor for CPU0
- End-to-End ECC protection on all matrix related access paths
- Safety Test Control Unit (STCU) for Logic BIST (LBIST) and Memory BIST (MBIST) controller
- One Interface Safety Monitor (ISM) module to monitor up to 32 delays/periods/duties of critical signals
- One Interrupt Monitor (INTM) module; supports up to 4 channels and can monitor the interrupt keep-active timeout or interrupt generation timeout
- CM7 core self-test API in ROM code

- **Timers**
  - Up to eight Flexible Timer Unit (FTU) modules with IC/OC/PWM function; FTU2/3 also support Quadrature Decoder function and 24bit count
  - One Timer Process Unit (TPU) with up to 32 channels. Two 24-bit count TCR1/2. TCR2 also supports angle count mode. Each channels support 2 matches compare and 2 capture
  - One Always-on Timer (AONTIMER) with standby wake up capability
  - Two Programmable Timers (PTIMERs)
  - One FC Programmable Interrupt Timers (FCPIT); each has 4 channels
  - One Real-Time Clock (RTC)
  - Up to two 56-bit Timer Stamps (TSTMPs) with four 32-bit compare channels, TSTMP0 runs at 1 MHz clock and TSTMP1 runs at Bus clock
  - One Frequency Measurement (FREQM) Module; with up to 64 input clock sources
- **Package**
  - 176LQFP-EP, 144LQFP-EP and 100LQFP-EP package options

2.2 Feature Comparison

The table below lists the major features and peripheral counts of the FC7240F2MDS devices.

Table 1. FC7240F2MDS feature list

Features				Chip
				FC7240F2MDS
Automotive cert.	Temp.Grade			Grade1/ -40°C to +125°C
Function Safety				ASIL-D
Power Design	Voltage Range			3.0V to 5.5V
	T_A			-40°C to +125°C
	T_J			-40°C to +150°C
CPU	Core			Cortex-M7; 1*Lockstep
	Frequency			240 MHz
	MPU			Yes
	I CACHE			16 KB
	D CACHE			8 KB
Memory	PFlash			2 MB
	DFlash			128 KB
	RAM	SRAM		96 KB
		TCM		192 KB
	ROM			128 KB
Clock				Multi clocks, including FIRC96M/SIRC12M/SIRC32K/FOSC48M/SOSC32K/PLL
Digital IOs				152
Peripherals	System	CPM		Yes
		DMA		1 × 16-channel
		WKU		Yes
		PMC		Yes
		SMC		Yes
		RGM		Yes
		SEC		Yes
		CORDIC		Yes
		CSC		Yes
		SCM		Yes
		MAM		Yes
		MB		Yes
	Memory	FMC		Yes
		ACC		Yes
		OSPI		No
	Clocking	SCG		Yes
		PCC		Yes
	Function Safety	WDOG		2
		EIM		Yes

Features			Chip
			FC7240F2MDS
Peripherals	Function Safety	ERM	Yes
		INTM	Yes
		CMU	5
		ISM	Yes
		FCSMU	Yes
		STCU	Yes
	Security	CRC	Yes
	HMI	GPIO	Yes
		PORT	Yes
		TRGSEL	6
		LU	Yes
	Analog	ADC	2
		CMP	2
		TMU	Yes
	Timer	FTU	8
		FCPIT	Yes
		TSTMP	2
		RTC	Yes
		AONTIMER	Yes
		PTIMER	2
		FREQM	Yes
		TPU	Yes
	Comm.	FCSPI	6
		FCIIC	2
		FCUART	8
		FLEXCAN	4
		SENT	Yes
		SDDF	No
		MSC	Yes
		ENET	No
Security			HSM, EVITA Full
Package		176LQFP-EP	Yes
		144LQFP-EP	Yes
		100LQFP-EP	Yes

Revision History

Revision	Date	Changes
0.1	2023/07/14	Initial release
0.1.1	2023/08/14	Fixed typos by changing the TCM size from "160 KB" to "192 KB"

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